ETU 721 CMOS DESIGN Question Bank (Dr P R Deshmukh)

1. List the steps in CMOS fabrication process?
2. Elborate VLSI Design Flow?
3. Explain the operation of nMOS /pMOS Enhancement Transistor?
4. Explain the operation of nMOS /pMOS Depletion Transistor?
5. Discuss the CMOS Technology related following process:
    - Wafer formation
    - Photolithography
    - Well and channel formation
    - Silicon Dioxide, Gate Oxide
    - Isolation
    - Gate and Source/Drain formation
    - Contact and Metallization
6. Write a short notes on λ layout design rules?
7. Why layout rules are essentials for fabrication of CMOS IC?
8. Elborate Design rules : Well rules, Transistor rules, Contact rules, Metal rules, Via Rules
9. Define threshold voltage of Transistor? Elaborate the parameter which will effect the threshold voltage?
10. Explain I-V / C-V characteristics of MOS Transistor?
11. Explain velocity saturation and mobility degradation (non ideal I-V Effect) ?
12. Elborate D-C Transfer characteristics of CMOS Inverter?
13. Derive the expression for Tranconductance(g_m) and output conductance (g_{ds})?
14. Describe Body effect?
15. Describe short channel effect? Or Explain channel length modulation?
16. Explain mobility variation in MOS Transistor?
17. Describe Fowler-Nordheim (F.N.) tunnelling with regards to MOS Transistor?

18. Describe CMOS transmission gate?
19. Describe 2 to 1 / 4 to 1 Multiplexer using Transmission Gate?
20. Describe CMOS Positive level senstitive / positive edge trigeer filpflop ?
21. Implement a 4:1 Mux using only CMOS Logic gates?
22. Implement CMOS Logic gates for following functions

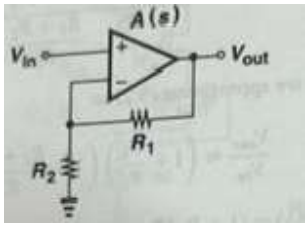
$Y = \overline{(A.B. + C.D) . E}$ $Y = \overline{(A.B.C.D.)}$ $Y = \overline{AB+(A+B)C}$

$F = A\,\underline{B} + \underline{A}\,B$

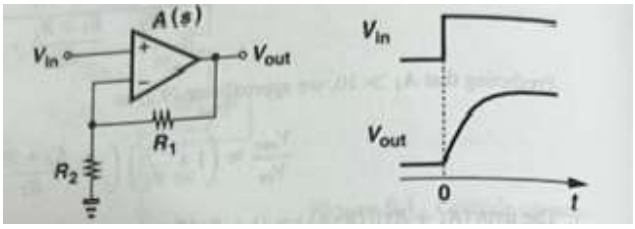
23. Elaborate Typical Read and Write dynamic RAM Architecture?
24. Explain CMOS and ECL conversion process using BiCMOS?
25. List the features of BiCMOS Technology?
26. Explain the working of BiCMOS Inverter?
27. Explain the working of BiCMOS 2-Input NOR Gate?
28. Explain the working of BiCMOS 2-Input NAND Gate?

29. Explain the working of BiCMOS column sense amplifier for high speed memory array?
30. Design a BiCMOS circuit to implement function Z = AB + C

31. Elaborate MOS small signal model?
32. List the steps in Analog design steps?
33. Describe common source stage? (with resistive load/diode connected load/Current source load/triod load)
34. Describe common Gate stage?
35. Describe cascode stage?
36. Elaborate Qualitative analysis of differential pair Amplifier?
37. Describe the concept of current mirrors in Analog CMOS Design?
38. Describe the concept of current sources in Analog CMOS Design?
39. Describe small signal analysis for diffrentail pair with active current mirror ?
40. A circuit of Non-inverting OP-Amp is designed for nominal gain of 10 i.e. 1+R2/R1 =10. Determine the minimum value of Gain A for the gain error of 1 % ?



41. In the circuit assume the op-amp in single pole voltage amplifier. If Vin is small step,



Calculate the time required for the output voltage to reach with in 1 % of its final value. What is unit gain bandwidth must the op-amp provide if 1+ R1/R2 =10 (nearly equal) and settling time less than 5 ns. For simplicity assume low frequency gain is much greater than unity.

42. Describe two stage implementation of op-amp?
43. Elaborate the Gain Boosting design issues in operational op-amp?
44. A n MOS Transistor is operated in triode region with following parameters

Vgs = 4 V , Vtn = 1 V, VdS = 2 V , W/L= 100, μ_n *Cox = 90 uA/v^2

Find drain current and Drain to source resistance?

45. Find g_m and R_{DS} for n channel transistor with Vgs= 1.2 V , Vtn= 0.8 V , W/L = 10, μ_n *Cox = 92 uA/v^2 and Vds = Veff + 0.5 V , Lambda = 0.953 per volt

46. Consider the process technology with following parameters

Oxide thickness tox = 9.5 nm

Mobility (Electron) = 540 cm ^{2} / V per sec

Mobility (Holes) = 220 cm ^{2} / V per sec

Wn = Wp = 12 µm

Ln=Lp= 0.35 µm

Vin = 0.65 V

| Vtp | = 0.74 V

Gate Voltage Vgs = 3.3 V

Calculate the value of Rn and Rp of two FETS

Assume €o = 8.85 * $10^{-14}\ F/cm$

47. Enhancement mode Nmos and Pmos device both have parameters L= 4 µm and tox= 500 ^{0}A. for the Nmos transistor Vtn = +0.6 V , µn = 675 cm^2/v/Sec , and the channel width is Wn. For PMOS transistor µp= 375 cm^2/v/Sec and channel width is Wp. Design the width of two transistors such that they are electrically equivalent and the drain current in the pmos transistor is I_D= 0.8 mA, when it is biased in saturation region at Vsg= 5 V. Calculate the values of $\beta p, \beta n, Wp, Wn$?