ETU 725 VLSI DESIGN Question Bank (Dr P R Deshmukh)

1. Explain the operation of nMOS /pMOS Enhancement Transistor?
2. Explain the operation of nMOS /pMOS Depletion Transistor?
3. Describe CMOS transmission gate?
4. Describe 2 to 1 / 4 to 1 Multiplexer using Transmission Gate?
5. Describe CMOS Positive level senstitive / positive edge trigeerfilpflop ?
6. List the steps in CMOS fabrication process?
7. Elborate VLSI Design Flow?
8. Implement a 4:1 Mux using only CMOS Logic gates?
9. Implement CMOS Logic gates for following functions

   $Y = \underline{(A.B + C.D).E}$, $Y = \underline{(A.B.C.D)}$, $Y = \underline{AB + (A+B)C}$, $F = \underline{a.b + \underline{a\,b}}$

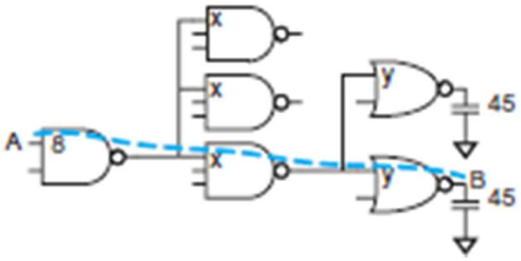
   $F = A.\underline{B} + \underline{A}.B$

10. Define threshold voltage of Transistor? Elaborate the parameter which will effect the threshold voltage?
11. Explain I-V / C-V characteristics of MOS Transistor?
12. Explain velocity saturation and mobility degradation (non ideal I-V Effect) ?
13. Elborate D-C Transfer characteristics of CMOS Inverter?
14. Explain the concept of switch level RC Delay model?
15. Describe Body effect?
16. Describe short channel effect? Or Explain channel length modulation?
17. Explain mobility variation in MOS Transistor?
18. Describe Fowler-Nordheim (F.N.) tunnelling with regards to MOS Transistor?
19. Explain concept of Impact ionization?
20. Derive the expression for Tranconductance(g_m) and output conductance (g_{ds})?
21. Write a short note on Figure of merit?
22. Derive the basic DC equation of MOS transistor in 3-Regions?
23. Calculate the threshold voltage for N-transistor at 300^0 k for a process with Si substrate with $N_A = 1.8 * 10^{16}$ cm^{-3}, A SiO_2 gate oxide thickness (t_{ox}) 200 A^0,
    Assume $\phi_{ms} = -0.9$ v, $Q_{fc}=0$,
    $N_i = 1.4 * 10^{10}$ cm^{-3}, $\epsilon_{ox} = 3.9$, $\epsilon_o = 8.85 * 10^{-14}$ f/cm, $\epsilon_{si} = 11.7 * \epsilon_o$,
    $\frac{KT}{q} = 0.02586$ v, $q = 1.6 * 10^{-19}$
24. Typical values for n device transistor for current process are as
    $\mu_n = 500$ cm^2/Vsec , $\mu_p = 180$ cm^2/Vsec, $\epsilon_{ox} = 3.9 * \epsilon_o$,
    $\epsilon_o = 8.85 * 10^{-14}$ f/cm, $t_{ox} = 200$ A^0 calculate ratio $\frac{\beta n}{\beta p}$
25. Explain the effect of $\frac{\beta n}{\beta p}$ ratio on the transfer characteristics of CMOS Transistor?
26. Write a short notes on noise margin in CMOS inverter?

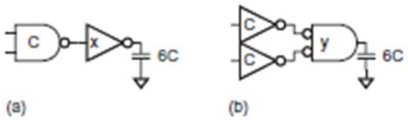
27. Calculate the Noise Margin for a CMOS inverter operating at 3.3 v(Vdd) , Vth=0.7v, Vtp=-0.7v, $\beta p = \beta n$

28. Write a short notes on λ layout design rules?
29. Why layout rules are essentials for fabrication of CMOS IC?
30. Draw a stick diagram for
    Inverter, 2input NAND /NOR gate
31. Discuss the CMOS Technology related following process:
    - Wafer formation
    - Photolithography
    - Well and channel formation
    - Silicon Dioxide, Gate Oxide
    - Isolation
    - Gate and Source/Drain formation
    - Contact and Metallization
32. Elborate Design rules : Well rules, Transistor rules, Conatct rules, Metal rules, Via Rules
33. Elborate CMOSPrcoess Enhancement Issues :
    - silicon on insulator concept
    - Mutiple Threshold voltages and Oxide Thickness
    - Interconnect
    - Circuit Elements
34. Elborate Technology related CAD Issues:
    - Design Rule Checking (DRC)
    - Circuit Extraction

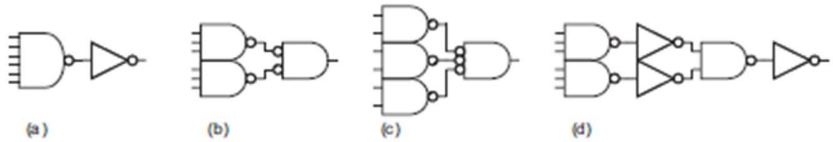
35. Describe capacitance of MOS Transistor OR Explain capacitance estimation of MOS device indicating accumulation, depletion, transistor and its variation with V_{gs}.
36. Derive the expression for Rise Time, Fall time, delay time?
37. Write a short note on Resistance Estimation?
38. Discuss Design Margin guidelines in CMOS?
39. Discuss Reliability issues in CMOS?
40. Elaborate Latchup issue in CMOS?
41. Eloborate Elmore Delay model?
42. Write a short note on Linear Delay Model?
43. Discuss logical efforts and Transistor sizing issues in delay calculations?
44. A ring oscillator constructed from odd number of oscillators , Estimate the frequency of N-stage ring oscillator?
45. Estimate minimum delay from A to B, find the value of X and Y



46. Estimate delay of fanout 4 of an inverter (inverter driving 4 identical copies). Assume unit/reference size inverter (aspect ratio pMOS = 2, Nmos=1)
47. Define Logical effort, Branching effort, effort delay,parasitic delay with reference to delay calculations?
48. Discuss Interconnect Geometry issues in CMOS circuits?
49. What is transistor sizing? why it is necessary ?OR Write a short note on transistor sizing?
50. Explain in Brief Total power dissipation in CMOS Circuits?
51. Explain in Brief Dynamic power dissipation?
52. Explain in Brief Static power dissipation?
53. Elaborate the various methods by which power dissipation can be minimized?
54. Discuss the scheme to drive big capacitive load?
55. Consider the nMOS transistor in a 65 nm process with a nominal threshold voltage of 0.3 V and a doping level of 8 × 1017 cm–3. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 0.6 V instead of 0?
56. Consider the two designs of a 2-input AND gate shown in Figure. Give an intuitive argument about which will be faster. Back up your argument with a calculation of the path effort, delay, and input capacitances x and y to achieve this delay.

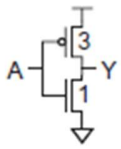


57. Consider four designs of a 6-input AND gate shown in Figure. Develop an expression for the delay of each path if the path electrical effort is H. What design is fastest for H = 1? For H = 5? For H = 20? Explain your conclusions intuitively.



58. An output pad contains a chain of successively larger inverters to drive the (relatively) enormous off-chip capacitance. If the first inverter in the chain has an input capacitance of 20 fF and the off-chip load is 10 pF, how many inverters should be used to drive the load with least delay? Estimate this delay, expressed in Fanout 4 inverter delays.

59. Consider a process in which pMOS transistors have three times the effective resistance as nMOS transistors. A unit inverter with equal rising and falling delays in this process is shown in Figure . Calculate the logical efforts of a 2-input NAND gate and a 2-input NOR gate if they are designed with equal rising and falling
delays.



60. You are considering lowering VDD to try to save power in a static CMOS gate. You will also scale Vt proportionally to maintain performance. Will dynamic power consumption go up or down? Will static power consumption go up or down?

61. Compute the sheet resistance of a 0.22 µm thick Cu (copper) wire in a 65 nm process. Find the total resistance if the wire is 0.125 µm wide and 1 mm long with Resistivity of Cu = $2.2 \times 10^{-8}\,\Omega \cdot \mathrm{m}$
62. Explain the concept of TAP Controller?
63. Elaborate the concept of Boundary Scan? state the difference between
64. Discuss the Boundary Scan Description Language?
65. Write a short note on Design of Testability?

Teacher Assessment

Project Gr No	Above Question sr No
1	1,2,10,11,28,34,64,65,27,26
2	3,4,11,12,30,31,33,37,38,63
3	5,6,13,14,32,32,60,61,62,7
4	7,8,,15,16,33,34,58,59,58,65
5	9,1,17,18,19,29,54,55,56,57
6	9,39,40,41,42,26,27,51,52
7	45 to 50, 30 to 34
8	21 to 27, 44,43,42
9	36 to 41, 22,23,25,8
10	33,34,58,59,58,65,7,8,,15,16,
11	32,60,61,62,7,5,6,13,14,33,
12	31,33,37,38,63,3,4,11,12,30
13	1,10,28,35,2,11,29,36,9,27
14	9,27,34,65,3,13,30,37,15,16
15	7,14,31,28,38,44,27,8,3
16	5,15,33,40,8,26,29,64,6,50
17	28 to 24, 9,27,65,22
18	65,7,8,,15,16,33,34,58,59,58
19	41 to 50
20	34,64,65,27,26,1,2,10,11,28
21	30 to 34,45 to 50
22	5,6,13,61,62,7,14,32,32,60
23	31,33,37,61,62,3,4,11,12,30
24	30 to 34, 51 to 55
25	3 to 7, 61 to 65
26	15 to 20, 34,39,66,48,40