"Towards Global Technological Excellence"

GOVERNMENT COLLEGE OF ENGINEERING, AMRAVATI

A Seminar Report on

Low Power Design Techniques in VLSI

Submitted to Government College of Engineering, Amravati for the partial fulfilment of requirements of degree of Bachelor of Technology

in

Electronics and Telecommunication Engineering

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CERTIFICATE

This is to certify that the seminar report entitled

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to Government College of Engineering, Amravati for the partial fulfilment of requirements of degree of Bachelor of Technology in Electronics and Telecommunication Engineering, is a bonafide record of the seminar work carried out by him/her under my guidance and supervision. This report in any form has not been submitted to any other institute for any purpose.

Dr. P. R. Deshmukh
(Guide & Head)

DECLARATION

We **Kartik Suhas Deogade, Sanket Gopichand Meshram, Sudhanshu Arun Wankhede** hereby declare that the seminar report on **Low Power Design Techniques in VLSI**, submitted for partial fulfilment of the requirements for the award of degree of Bachelor of Technology of the Government College of Engineering. Amravati is a bonafide work done by me under supervision of **Dr**. **P. R. Deshmukh.**

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ACKNOWLEDGEMENT

In this part of report we like to express my deep sense of gratitude and sincere thanks to all those illumination because of whom, this work has become successful. We are highly Indebted to **Dr. P. R. Deshmukh** for her guidance and constant supervision as well as for providing necessary information regarding the seminar and also for her support in completing the report successfully.

We would like to express my special gratitude and thanks to our Respected Head of Department, **Dr. P. R. Deshmukh** for giving us such attention and time. We also acknowledge and thank to our Honorable Principal **Prof. Dr. A. M. Mahalle** and all the staff members of Electronics and Telecommunication Department who has directly and indirectly helped in completing the seminar report.

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Abstract

Low power has emerged as a principal theme in today's world of electronics industries. Power dissipation has become an important consideration as performance and area for VLSI Chip design. With shrinking technology reducing power consumption and over all power management on chip are the key challenges below 100nm due to increased complexity. For many designs, optimization of power is important as timing due to the need to reduce package cost and extended battery life. For power management leakage current also plays an important role in low power VLSI designs. Leakage current is becoming an increasingly important fraction of the total power dissipation of integrated circuits. This paper describes about the various strategies, methodologies and power management techniques for low power circuits and systems. Future challenges that must be met to designs low power high performance circuits are also discussed.

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1. Introduction

The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before. Requirements for lower power consumption continue to increase significantly as components become battery-powered, smaller and require more functionality. In the past the major concerns for the VLSI designers were area, performance and cost. Power consideration was the secondary concerned. Now a day's power is the primary concerned due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption. The motivations for reducing power consumption differ application to application. In the class of micro-powered battery-operated portable applications such as cell phones, the goal is to keep the battery lifetime and weight reasonable and packaging cost low. For high performance portable computers such as laptop the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation. Finally for the high performance non battery-operated system such as workstations the overall goal of power minimization is to reduce the system cost while ensuring long term device reliability. For such high-performance systems, process technology has driven power to the fore front to all factors in such designs. At process nodes below 100 nm technology, power consumption due to leakage has joined switching activity as a primary power management concern. There are many techniques [1] that have been developed over the past decade to address the continuously aggressive power reduction requirements of most of the high performance. The basic low-power design techniques, such as clock gating for reducing dynamic power, or multiple voltage thresholds (multi-Vt) to decrease leakage current, are well-established and supported by existing tools [2].

2. Literature Survey

The continuing demand for higher performance and smaller form factors in electronic devices has necessitated the development of low power design techniques in Very Large-Scale Integration (VLSI). As devices become increasingly miniaturized, power consumption has become one of the most critical design constraints. The need for low power designs is driven by several factors including energy efficiency, thermal management, portability, and battery life, particularly for mobile and IoT devices. This literature review surveys the most relevant low-power design techniques in VLSI, focusing on circuit, architectural, and system-level approaches.

2.1 Power Dissipation in VLSI

Power dissipation in CMOS circuits comes from two components:

Dynamic dissipation due to

- charging and discharging load capacitances as gates switch
- "short-circuit" current while both pMOS and nMOS stacks are partially ON

Static dissipation due to

- subthreshold leakage through OFF transistors
- gate leakage through gate dielectric
- junction leakage from source/drain diffusions
- contention current in ratioed circuits

Putting this together gives the total power of a circuit [3]:

$$P_{\text{dynamic}} = P_{\text{switching}} + P_{\text{short circuit}}$$
$$= \alpha C V_{DD}^2 f$$

$$P_{\text{static}} = \left(I_{\text{sub}} + I_{\text{gate}} + I_{\text{junct}} + I_{\text{contention}} \right) V_{DD}$$

$$P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}}$$

Where

C_L: Load Capacitance, a function of fan-out, wirelength, and transistor size,

V_{dd}: Supply Voltage, which has been dropping with successive process nodes,

α: Activity Factor, meaning how often, on average, the wires switch,

f: Clock Frequency, which is increasing at each successive process node.

Static power or leakage power is a function of the supply voltage (V_{dd}), the switching threshold (Vt), and transistor sizes.

As process nodes shrink, leakage becomes a more significant source of energy use, consuming at least 30% of total power [3]. Crowbar currents, caused when both the PMOS and NMOS devices are simultaneously on, also contribute to the leakage power dissipation [2]. Most circuit level minimization techniques focus only on Sub threshold leakage reduction without considering the effects of gate leakage [1].

2.2 Low Power Design Space

From the above section it is revealed that there are three degrees of freedom in the VLSI design space: Voltage, Physical Capacitance and data activity. Optimizing for more power entails an attempt to reduce one or more of these factors. This section briefly describes about their importance in power optimization process.

1. Voltage: - Because of its quadratic relationship to power, voltage reduction offers the most effective means of minimizing power consumption. Without requiring any special circuits and technologies, a factor of two reduction in supply voltage yields a factor of four decreases in power consumption. Unfortunately, there is speed penalty for supply voltage reduction and delays drastically increase as Vdd approaches to the threshold voltage Vt of the device. The approach to reduce the supply voltage without loss in throughput is to modify the threshold voltage of the devices. Reducing the Vt allows the supply voltage to be scaled down without loss in speed. The limit of how low the Vt can go is set by the requirement to set adequate noise margins and control the increase in the subthreshold leakage current [4,5,6].

2. Physical Capacitance: -Dynamic power consumption depends linearly on the physical capacitance being switched. So, in addition to operating at low voltages, minimizing

capacitances offer another technique for minimizing power consumption. The capacitances can be kept at a minimum by using less logic, smaller devices, fewer and shorter wires [4,5,6]. As with voltage, however, we are not free to optimize capacitances independently, for example reducing device sizes reduces physical capacitance, but it also reduces the current drive of the transistor making the circuit operate more slowly.

3.Switching Activity: -There are two components to switching activity: Fclk which determines the average periodicity of data arrivals and E(sw) which determines how many transitions each arrival will generate [7]. E(sw) is reduced by selecting proper algorithms architecture optimization, by proper choice of logic topology and by logic level optimization which results in less power [1]. The data activity E(sw) are combined with the physical capacitance C to obtained switch capacitance Csw=C.E(sw), which describes the average capacitance charge during each data period1/Fclk which determines the power consumed by CMOS circuit [8].

3. Methodologies

3.1 Supply Voltage Scaling

Voltage has a quadratic effect on dynamic power. Therefore, choosing a lower power supply significantly reduces power consumption. As many transistors are operating in a velocity-saturated regime, the lower power supply may not reduce performance as much as long-channel models predict. The chip may be divided into multiple voltage domains, where each domain is optimized for the needs of certain circuits.[3]

In VLSI, power consumption is composed of two main types: **dynamic power** and **static (or leakage) power**. Dynamic power is primarily due to the switching activity in transistors and can be reduced effectively by decreasing the supply voltage. The relationship of dynamic power consumption with supply voltage can be expressed by the equation:

$$P_{dynamic} = \alpha C V_{DD}^2 f$$

where:

- α is the switching activity factor,
- C is the load capacitance,
- V_{DD} is the supply voltage, and
- f is the operating frequency.

In this equation, power consumption is proportional to the square of the supply voltage (V_{dd}^2). Therefore, a 10% reduction in V_{dd} can reduce dynamic power by roughly 19%, making supply voltage scaling a highly effective means of power reduction.

Voltage also can be adjusted based on operating mode; for example, a laptop processor may operate at high voltage and high speed when plugged into an AC adapter, but at lower voltage and speed when on battery power. If the frequency and voltage scale down in proportion, a cubic reduction in power is achieved. For example, the laptop processor may scale back to 2/3 frequency and voltage to save 70% in power when unplugged.[3]

3.2 Challenges in supply voltage scaling

A factor of two reduction in supply voltage yields a factor of four decrease in energy.

Theoretical lower limit of supply voltage of CMOS circuit is 0.2V.

As supply voltage is lowered delay increases leading to dramatic reduction in performance.

Objective of SVS is to scale supply voltage without compromise performance.[9]

Overall, while supply voltage scaling is effective for reducing power, it requires careful management ofperformance, reliability, and design trade-off.

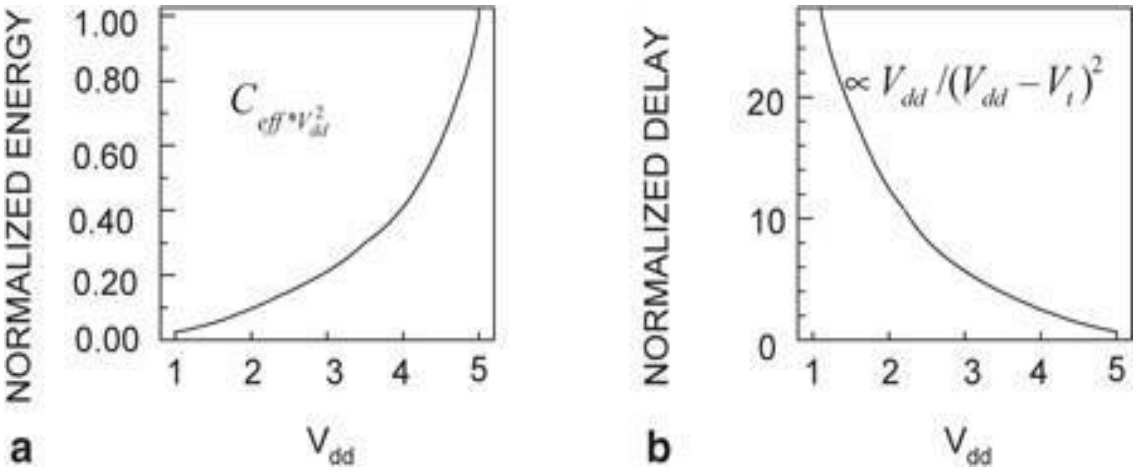

Figure 3.1: Relation between Energy and Delay

3.3 Constant Field Scaling in VLSI Design

Constant field scaling is a classical approach in VLSI design used to achieve transistor miniaturization while maintaining or improving performance and reducing power consumption. As transistor sizes shrink with each new technology node, constant field scaling ensures that the electric field within a transistor remains approximately constant, thereby preserving device reliability and preventing performance degradation due to excessive electric fields. This method has been widely used in the semiconductor industry to enable smaller, faster, and more power-efficient devices.

The principle of constant field scaling is straightforward: when transistor dimensions (e.g., channel length, width, and oxide thickness) are scaled down by a factor, SSS, other associated parameters (such as supply voltage V_{dd}, threshold voltage Vth, and doping concentrations) are also scaled to ensure that the electric field across the transistor remains unchanged. This keeps the device behavior consistent with the original design, allowing it to operate reliably despite its reduced size.

3.3.1 Key Parameters in Constant Field Scaling

In constant field scaling, all critical device parameters are scaled by the same factor, SSS, according to the following rules [9]:

1. **Linear Dimensions**: Channel length, width, and oxide thickness are scaled by 1/S.
2. **Supply Voltage** (V_{dd}): Scaled by 1/S, reducing the power consumption.
3. **Doping Concentration**: Scaled by S to ensure that threshold voltage and other electrical characteristics are preserved.
4. **Threshold Voltage** (Vth): Scaled by 1/S, maintaining consistent transistor switching characteristics.

This systematic scaling of parameters ensures that the internal electric field (EEE) within the transistor remains nearly constant.

$$E = V_{dd} / L$$

where L is the channel length. By scaling V_{dd} and L proportionally, E remains unchanged, preventing excessive electric fields that could otherwise lead to reliability issues like hot carrier effects or oxide breakdown.

3.3.2 Benefits of Constant Field Scaling

1. Reduced Power Consumption: Since power consumption is proportional to the square of the supply voltage (V_{dd}), scaling down V_{dd} reduces dynamic power significantly.
2. Higher Device Density: By scaling down the transistor dimensions, more devices can be packed into a given area, leading to higher circuit density and more complex integrated circuits.
3. Improved Performance: Smaller transistor dimensions reduce parasitic capacitances and enable faster switching speeds, enhancing the overall speed of the circuit.
4. Maintained Device Reliability: By keeping the electric field constant, constant field scaling reduces the risk of device degradation over time, thus maintaining long-term reliability.

3.4 Clock Gating in VLSI Design

The commonly used register transfer level (RTL) in the optimization of the reduction of the power dynamics is the Clock gating [10]. This is because this technique is only applied to the clock modules which instantly working by providing the additional support to the currently existing synchronous circuits in pruning the clock tree thus shutting down the power consumption for the idle circuit in the system. This adoption of this technique can help in the reduction of the dissipation of power in the clock distribution network.

3.4.1 How Clock Gating Works

In typical digital circuits, a clock signal is distributed to various flip-flops, latches, and registers. Even when certain parts of a circuit are idle (not processing data), these elements still receive the clock signal, resulting in power consumption due to unnecessary switching. Clock gating reduces this consumption by inserting logic

gates, typically an AND or OR gate, in the clock path. These logic gates selectively enable or disable the clock signal based on a control signal (known as the **enable signal**) that indicates whether a circuit block needs to be active or idle.[11]

The basic mechanism involves:

1. Clock Enable Signal: A control signal that determines if the clock should be delivered toaparticular block. When this signal is "low," the clock is disabled for that block, stopping unnecessary toggling.
2. Gating Logic: Usually an AND gate (for a positive-edge-triggered clock) or an OR gate (for a negative-edge-triggered clock), which gates the clock based on the enable signal.

When the control signal is set to "off" for a given block, the clock is gated (disabled), stopping any flip-flops or latches in that block from switching. This approach is effective in reducing dynamic power consumption, especially in large circuits with several functional blocks that operate at different times.

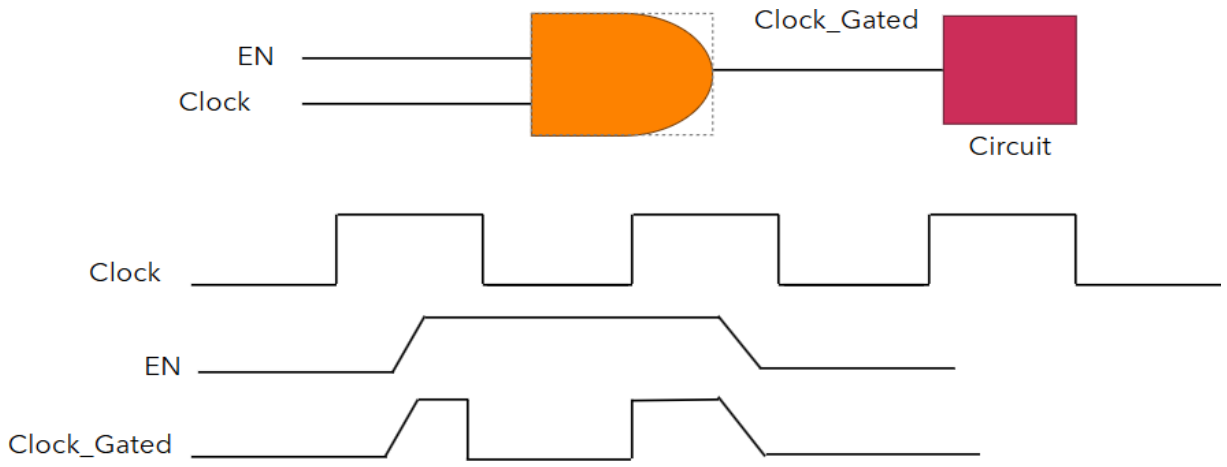

Figure 3.2: And Gate based clock gating

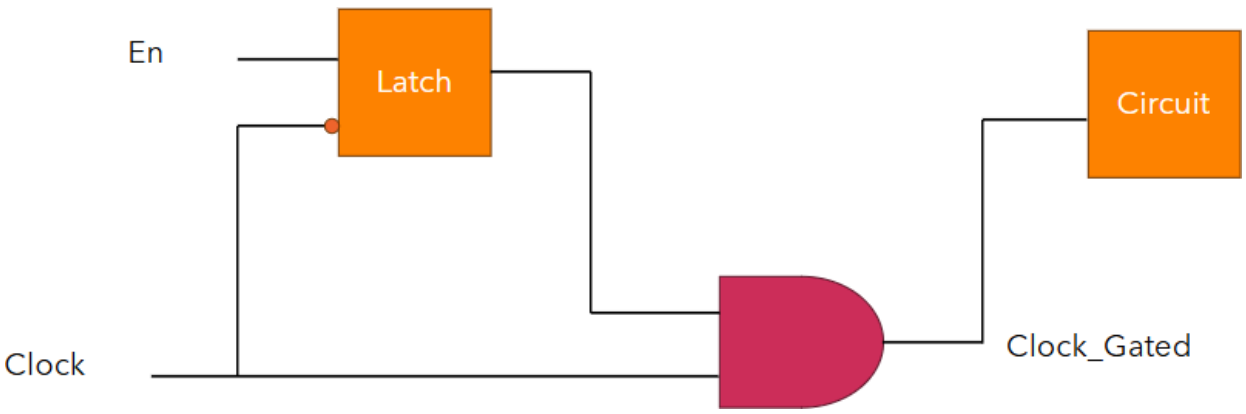

Figure 3.3: Latch based clock gating circuit

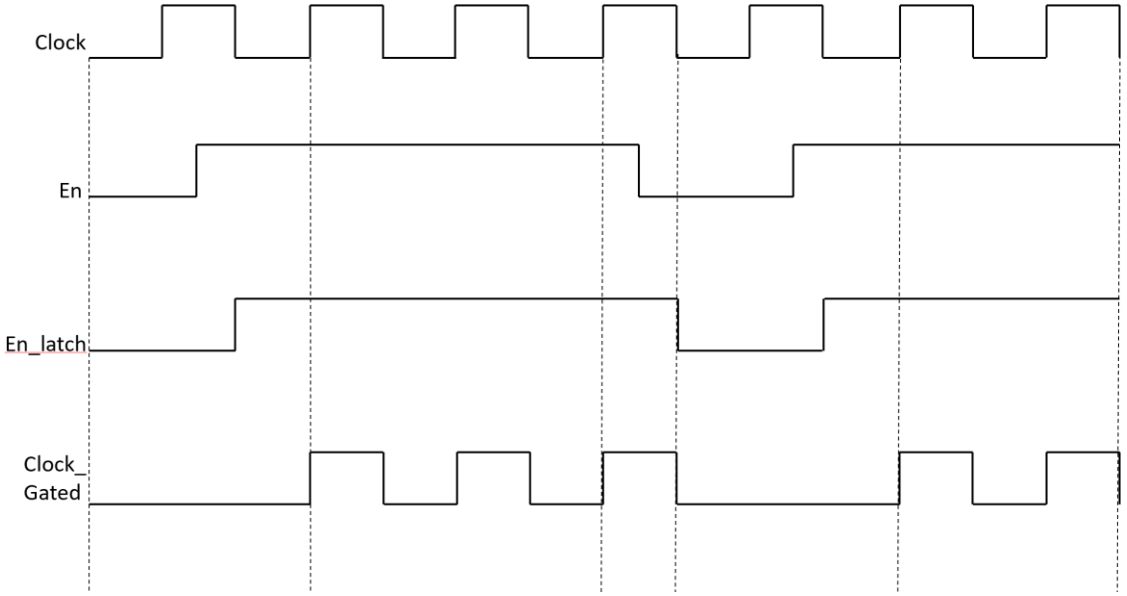

Figure 3.4: Latch based clock gating output

3.4.2 Types of Clock Gating

1. Synthesis-based Clock Gating: This is an automatic approach where the synthesis tools add clock gating logic based on opportunities identified in the design, such as redundant switching in registers. The tools analyze the circuit's logic to identify registers with enable conditions and replace them with gated clocks, reducing power without manual intervention from the designer.

2. Latch-based Clock Gating: This technique involves using a latch to hold the gating condition and applies it directly to the clock signal. A latch-based gate is often placed on

   the clock line to synchronize the clock signal with the enable signal, providing finer controland reducing any potential glitches.

3. Integrated Clock Gating Cells: Many modern VLSI libraries provide integrated clock gating cells that combine clock gating logic (such as AND/OR gates) with built-in glitch protection. These cells ensure a smooth gating process, making implementation easier andmore reliable.

3.4.3 Benefits of Clock Gating

1. Reduced Dynamic Power: Clock gating is one of the most effective techniques for reducing dynamic power, as it directly targets the main power-consuming signal in digital circuits.
2. Optimized Power Efficiency: By disabling clock signals to inactive circuit blocks, clock gating prevents unnecessary switching, resulting in lower overall power consumption.
3. Minimal Performance Impact: Clock gating can be applied without significant impact on circuit performance, as it only affects idle parts of the circuit while active components continue to operate normally.
4. Scalability: This technique can be applied across various levels, from individual flip-flops to larger modules, making it flexible for different design requirements.

3.5 Power Gating

During normal operation, SLEEP = 0. Both the PMOS and NMOS Sleep Transistors (in blue and green respectively) are ON. And we have Virtual Power Rails and Virtual Ground which ensure normal circuit operation.

However, during periods of low activity, SLEEP = 1. Hence the Sleep Transistors tum OFF. And a direct path from power rails to ground is broken and hence no leakage power is dissipated due to the Pull-up and Pull-down networks.

During normal operation, Sleep Transistors contribute to some extra leakage power because they are still ON. Though, the leakage power due to these two transistors would be extremely small compared to that of the Pull-up and Pull-down networks, nevertheless, these transistors are custom designed in a way such that they have high Vt (the threshold voltage) to reduce any excess leakage power during normal mode of operation.

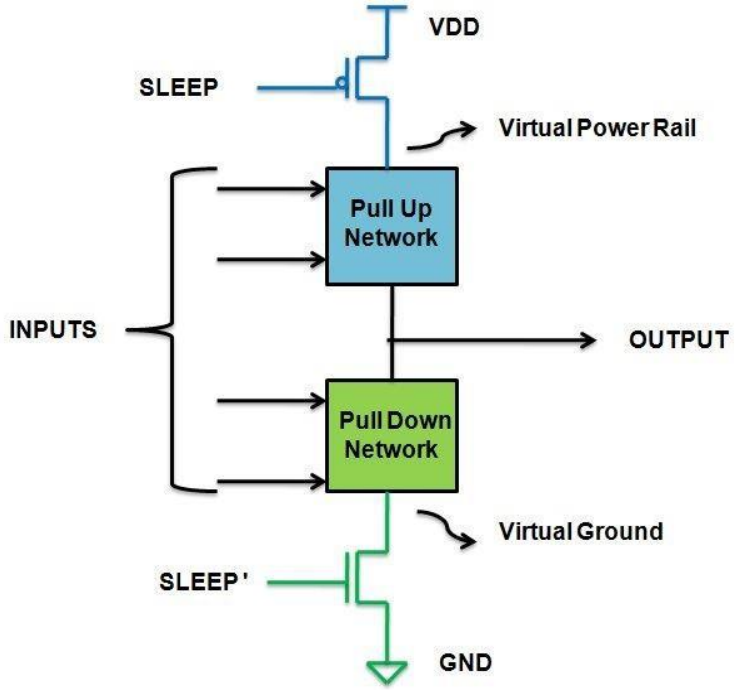

Figure 3.5: Basic power gating circuit

3.5.1 Working Phases of Power Gating

The easiest way to reduce static current during sleep mode is to turn off the power supply to the sleeping blocks. This technique is called power gating.[3]

The operation of power gating can be described in two phases: Power-on (Active mode) and Power-off (Sleep mode).

1. Power-on (Active Mode):In this mode, the sleep transistor is turned on, allowing the power supply (Vdd) to flow into the functional block of the circuit. The sleep transistor essentially acts as a low-resistance path, and the block operates as usual.

- PMOS Sleep Transistor (for Vdd side): The PMOS transistor will turn on when the gate voltage is low relative to the source, which is connected to Vdd. This allows current to flow from Vdd to the functional block.
- NMOS Sleep Transistor (for GND side): Similarly, an NMOS sleep transistor on the ground side turns on when the gate voltage is high relative to the source, enabling current flow to ground.

During the power-on state, the block is fully powered, and its functional circuits (logic gates, flip- flops, etc.) can perform normal operations.

2. Power-off (Sleep Mode)

In this mode, the sleep transistor is turned off. This creates an open circuit between the

power supply and the functional block, essentially cutting off the power to the block and reducing leakage currents.

- PMOS Sleep Transistor (for V_{dd}): When the gate voltage is high relative to the source, the PMOS transistor turns off, disconnecting the functional block from the power supply.
- NMOS Sleep Transistor (for GND): When the gate voltage is low, the NMOS transistor turns off, disconnecting the functional block from ground.

By turning off the power to the inactive block, leakage currents (the primary contributor to static power dissipation) are minimized, reducing the overall power consumption of the chip.

3.5.2 Controlling the Sleep Transistor

The sleep transistor is controlled by the sleep signal, which is typically generated by a power management unit. The signal can be:

- Active-low: In this case, when the sleep signal is low, the sleep transistor is turned on (power is supplied to the block). When the sleep signal is high, the sleep transistor is turned off (power is disconnected).
- Active-high: The behavior is reversed—when the sleep signal is high, the sleep transistor is onand power is supplied. When the signal is low, the transistor is turned off, disconnecting power.

This control mechanism ensures that only the necessary blocks are powered, and idle blocks are disconnected from the power supply.

3.5.3 Transition Between Active and Sleep Modes

The transition between active and sleep modes must be managed carefully to avoid issues like voltage glitches, which could affect the overall chip operation. The following actions are typically involved:

1. Power-on Sequence:
    - When the sleep signal is asserted to wake up a block, the sleep transistor gradually turnson.
    - To prevent inrush currents and potential voltage fluctuations, a gradual rise

in the gate voltage of the sleep transistor is used, especially if the block involves high-power devices.

2. Power-off Sequence:
    - When the block is going into sleep mode, the sleep transistor is gradually turned off. Care is taken to ensure that this happens when the block is not performing critical operations, avoiding potential glitches or unintended behavior.
3. Wake-up Delay:
    - When a block transitions from sleep to active mode, there is typically some wake-up latency, which is the time required for the sleep transistor to fully turn on and the block to resume normal operation. The wake-up time depends on the size of the sleep transistor, the block's characteristics, and any additional circuitry designed to mitigate wake-up delays.

3.6 Dynamic Voltage and Frequency Scaling (DVFS)

Dynamic Voltage and Frequency Scaling has emerged as a versatile technique for optimizing power consumption in processors. Initially employed in desktop and server environments, DVFS has garnered attention for its adaptability to the dynamic workload's characteristic of IoT devices. DVFS enables real-time adjustments to the operating voltage and frequency of a processor based on the current computational requirements. This dynamic tuning ensures that the processor operates at an optimal point on the power-performance curve, minimizing energy wastage during periods of low workload and maximizing performance during peak demand.[12]

DVFS is commonly used in processors (like CPUs, GPUs) and other integrated circuits to achieve power savings in mobile devices, laptops, servers, and other power-sensitive applications. By dynamically changing the voltage and frequency, DVFS can significantly reduce both dynamic power and static power consumption, helping to improve energy efficiency and extend battery life in portable devices.

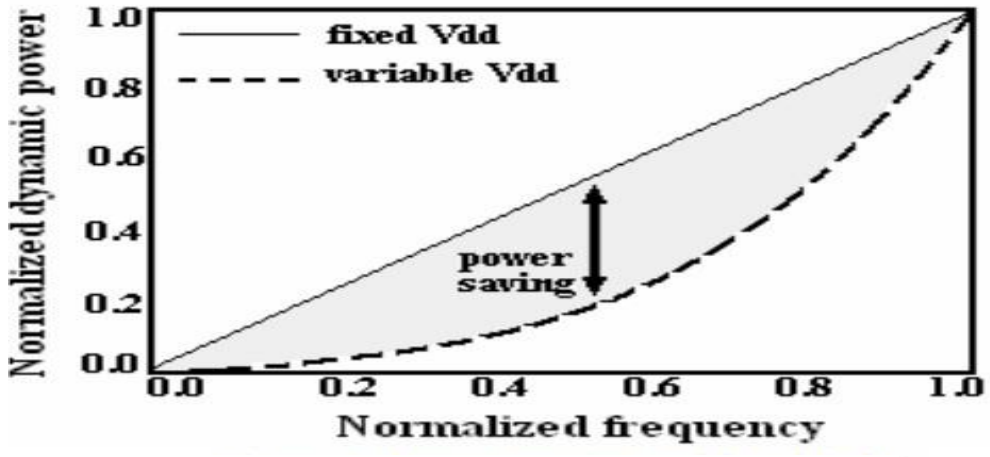

Figure 3.6: Power VS Frequency

3.6.1 How DVFS Works

DVFS works by scaling two key parameters:

1. Operating Frequency (f): The frequency at which the circuit operates (measured in Hz).
    - The frequency of operation controls how quickly a processor or circuit can performoperations.
    - Higher frequencies lead to higher performance, but also increase power consumptiondue to the increased number of switching events per unit time.
2. Supply Voltage (V_{dd}): The voltage that powers the circuit.
    - The power consumed by a digital circuit is proportional to both the frequency ofoperation and the square of the supply voltage.
    - Lowering the voltage reduces dynamic power consumption, but may also reduce theperformance capability.

3.6.2 Key Principles of DVFS

1. Power-Performance Tradeoff:
    - There is a tradeoff between power consumption and performance. Lowering the frequency and voltage reduces power consumption, but can also degrade performance (i.e., longer processing times).
    - DVFS allows the system to adjust this tradeoff based on the current

workload. During high-performance tasks, both frequency and voltage can be increased; during idle or less demanding tasks, they can be reduced to save power.

2. Dynamic Scaling:
    - DVFS allows the voltage and frequency to be adjusted in real-time based on the workload and performance requirements.
    - The scaling is often managed by a power management unit (PMU), which monitors the system's workload and adjusts voltage and frequency accordingly.

3.6.3 Benefits of DVFS

Several studies highlight the tangible benefits of integrating DVFS into the VLSI architecture of IoT devices. Improved power efficiency, extended battery life, and enhanced system reliability are among the key advantages observed. The adaptability of DVFS ensures that IoT devices can meet varying performance requirements while conserving energy during idle or low-demand periods. As a result, these devices can operate in remote or inaccessible locations for extended durations, making them more practical for diverse applications.[12]

3.6.4 Challenges and Limitations of DVFS

1. Trade-off between Power and Performance: Achieving an optimal balance between power efficiency and performance is a perpetual challenge. Aggressive power saving techniques might lead to a reduction in processing speed and overall system performance.
2. Dynamic Workload Variations: IoT applications often experience dynamic and unpredictable workloads. Designing a VLSI architecture that can efficiently adapt to these variations without sacrificing power efficiency poses a significant challenge.
3. Algorithmic Complexity: Implementing sophisticated power management algorithms, such as Dynamic Voltage and Frequency Scaling (DVFS), adds complexity to the design. Balancing algorithmic intricacy with hardware constraints is a challenge.
4. Reliability Concerns: Aggressive power-saving techniques, such as power gating, may introduce reliability concerns. The frequent activation and deactivation of components can lead to wear and tear, impacting the overall lifespan of the system.

5. Integration of Energy Harvesting: Integrating energy harvesting components, while beneficial for sustainability, introduces challenges related to the variability of energy sources and the need for efficient energy storage solutions.
6. Security Implications: Power-efficient designs may inadvertently introduce vulnerabilities. For instance, low-power modes might be exploited for side-channel attacks. Balancing security measures with power efficiency is a challenge.
7. Real-time Responsiveness: Achieving real-time responsiveness in power-efficient architectures can be challenging. Particularly in applications with stringent timing requirements, ensuring timely responses while minimizing power consumption requires careful consideration.[12]

3.7 Sleep Mode

Sleep mode is a widely used technique in VLSI (Very-Large-Scale Integration) design to minimize power consumption, particularly in systems where different components may be idle or inactive at various times. By selectively turning off power to specific components (or entire blocks) when they are not in use, sleep mode helps to significantly reduce static power (leakage) and sometimes dynamic power consumption. This is especially important for battery-powered and mobile devices, where energy efficiency is crucial.

3.7.1 Sleep Mode Types

Several sleep mode techniques can be used in VLSI design to reduce power consumption, including:

1. Idle Mode:
    - In idle mode, a block is not performing any useful computation but is still powered on. This is often used in communication systems, where a block might not be processing data but still needs to be ready for quick activation.
    - To reduce power consumption, clock gating or voltage scaling can be applied, effectively reducing the power consumption of the idle block.
2. Standby Mode:
    - In standby mode, the system is partially powered down, meaning that some

components of the circuit are turned off while others remain active. For instance, in multi-core processors, cores that are not actively processing data can be powered down while the active cores continue to function.

- Components like memory units or peripheral units may be put into low-power standby mode when not in use, ensuring that power consumption is minimized.

3. Deep Sleep Mode:

   - Deep sleep mode involves completely turning off power to certain sections of the circuit(or even the entire chip), resulting in the lowest possible power consumption.
   - During deep sleep, the system loses its state, and significant wake-up time may be required when it transitions back to active mode. This mode is particularly useful in battery-operated devices where extended power saving is needed, and immediate wake- up is not crucial.

4. Hibernate Mode:

   - Hibernate mode is similar to deep sleep but includes saving the system state to non- volatile memory (such as Flash or hard drive). This allows the system to "wake up" from hibernation and resume exactly where it left off. It's commonly used in devices where long-term power saving is required but quick recovery is not necessary.

3.7.2 Benefits of Sleep Mode in VLSI

1. Reduced Static Power:

   - Static power (mainly due to leakage currents) becomes a dominant factor as semiconductor technology scales down to smaller process nodes (like 7 nm, 5 nm). By turning off power to idle blocks or entire sections of the chip, sleep mode helps reduce these leakage currents and thus lowers overall power consumption.

2. Energy Efficiency:

   - Sleep mode allows components to conserve energy during idle periods. This is especially important for battery-powered devices such as smartphones,

laptops, and IoT devices, where saving power during inactive states directly contributes to longer battery life.

3. Thermal Management:
    - By turning off parts of the circuit that aren't needed, sleep mode can help reduce heat generation. This is critical in systems where thermal constraints are a concern, such as mobile devices or high-performance computing systems.
4. Improved Battery Life:
    - For mobile devices, reducing the power consumption during idle times through sleep modes extends the battery life significantly. Since the system only consumes full power when necessary, it can conserve energy when performing background tasks or while in idle states.
5. Increased System Longevity:
    - Reduced power consumption and heat generation can also improve the longevity of the system, as components experience less wear and tear due to thermal stress.

3.7.3 Challenges in Implementing Sleep Mode

1. Wake-up Latency:
    - One of the main challenges of using sleep mode is the wake-up latency. When a component is powered down, there can be a delay in returning to full functionality. This latency is the time it takes for the system to re-enable the power supply, re-initialize the block, and resume normal operations.
    - In time-sensitive applications, long wake-up times can be problematic. Therefore, minimizing wake-up latency is crucial, and this may require more complex power-management circuitry.
2. State Preservation:
    - When a block enters sleep mode, it may lose its current state (e.g., register contents, memory data), requiring mechanisms to save and restore the state

during transitions.

- Techniques like state retention (saving and restoring system states) or non-volatile memory can be used to mitigate this issue, but they introduce additional complexity.

3. Power Gating Complexity:

   - The design of sleep transistors and power gating logic adds complexity to the chip's architecture. It's crucial to ensure that the sleep transistors do not themselves consume significant power or add parasitic capacitance that may undermine the power-saving benefits of sleep mode.
   - The switching of these sleep transistors must also be handled carefully to avoid introducing noise, glitches, or power spikes that can affect the functionality of other active parts of the circuit.

4. System-Level Coordination:

   - Coordinating the power-down and power-up of multiple components requires a centralized power management unit (PMU) that can monitor the system's workload and determine when to enter and exit sleep modes.
   - The PMU must work closely with the operating system and application software to ensure that sleep modes are only engaged when the system can afford to enter low- power states.

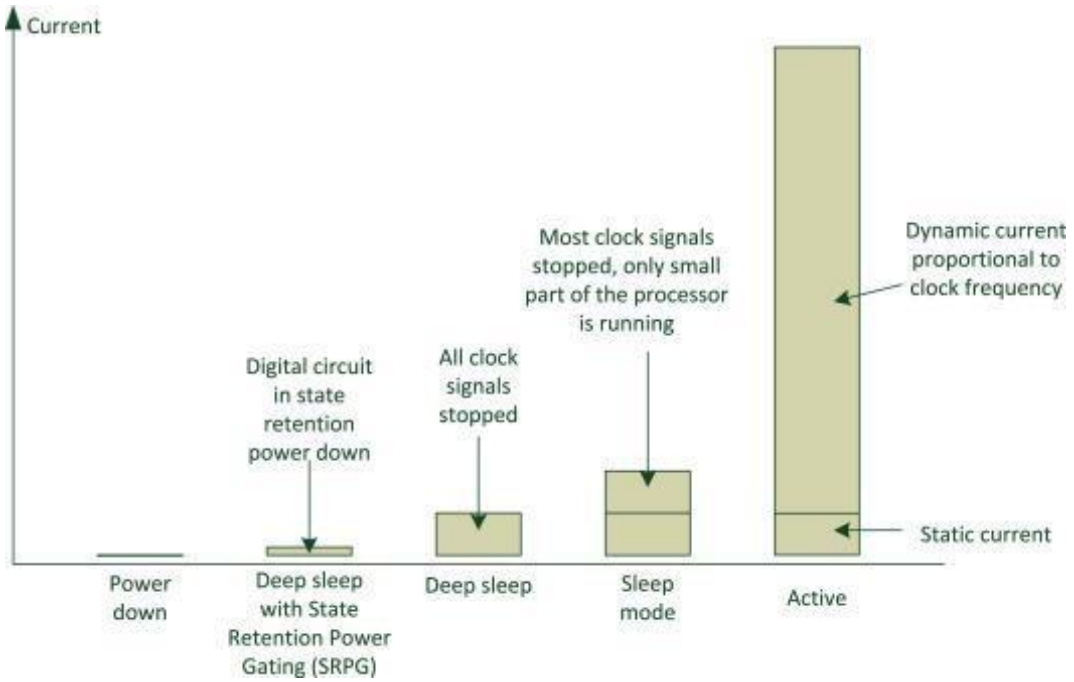

Figure 3.7: Different Sleep Modes

4. Applications

1. Clock Gating:
    - Applications: Microprocessors, FPGAs, embedded systems, SoCs.
    - Purpose: Reduces dynamic power by turning off clocks to inactive parts of the circuit.
2. Power Gating:
    - Applications: Multi-core processors, SoCs, mobile devices, high-performancecomputing.
    - Purpose: Cuts off power to unused blocks, reducing static leakage power.
3. Constant-Frequency Scaling:
    - Applications: Low-power embedded systems, real-time systems, IoT devices.
    - Purpose: Lowers voltage while keeping frequency constant, reducing powerconsumption.
4. DVFS (Dynamic Voltage and Frequency Scaling):
    - Applications: Mobile devices, laptops, servers, high-performance computing.
    - Purpose: Dynamically adjusts both voltage and frequency to optimize power andperformance.
5. Sleep Transistors:
    - Applications: Mobile devices, IoT devices, SoCs, wearables.
    - Purpose: Powers down inactive parts by isolating them from the power supply, savingleakage power.

5. Conclusion

The need for lower power systems is being driven by many market segments. Unfortunately designing for low power adds another dimension to the already complex design problem and the design has to be optimized for power as well as Performance and Area. In conclusion various issues and major challenges regarding low power designs are: -

1. Technology Scaling: - It relates with the following factors like: Capacitance per node reduces by 30%, Electrical nodes increase by 2X, die size grows by 14% (Moore's Law), Supply Voltage reduces by 15% and Frequency Increases by 2X. To meet these issues relatively 2.7 X active power will increase.
2. Leakage power: - To meet frequency demand Vt will be scaled which results high leakage power. A low voltage / low threshold technology and circuit design approach, targeting supply voltage around 1V and operating with reduced thresholds.
3. Dynamic power management techniques, varying supply voltage and execution speed according to the activity measurement.
4. Low power interconnect, using advance technology, reduced swing or activity approach.

5. Development of power conscious techniques and tools for behavioral synthesis, logic synthesis and layout optimization.

6. Power saving techniques that recycle the signal energies using the adiabatic switching principals rather them dissipating them as a heat and promising in certain applications where speed can be trades for low power.

6.Future Scope

1. Beyond CMOS Technologies: As traditional CMOS scaling hits physical limits, quantum computing, graphene, carbon nanotubes, and spintronics could enable ultra-low-power, high- performance systems.
2. AI-Driven Power Management: Machine learning can be used for dynamic, real-time power optimization, predicting workload patterns to adjust power and performance efficiently.
3. Neuromorphic Computing: Energy-efficient brain-inspired architectures for AI tasks will help reduce power consumption in intelligent systems, such as autonomous devices and robotics.
4. 3D ICs and Heterogeneous Integration: 3D chip stacking and integrating diverse processing units (e.g., CPUs, GPUs, AI accelerators) will optimize power and performance.
5. Low Power Wireless Communication: With the growth of IoT and 5G/6G, ultra-low-power wireless protocols and energy-harvesting technologies will become essential for maintaining long device lifetimes.
6. Energy-Efficient Memory: Low-power memory technologies like resistive RAM (ReRAM) andphase-change memory (PCM) will reduce power consumption in data storage and retrieval.
7. Hardware-Software Co-Design: Future systems will benefit from co-optimized software and hardware that works together to minimize power consumption across the entire system.

In essence, the future of low-power VLSI design will focus on leveraging new materials, AI, advanced process nodes, and energy-efficient communication to meet the increasing demand for power- conscious, high-performance electronic systems.

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